TOWARDS REAL TIME REMOTE SENSING LABORATORY: IMAGE ENHANCEMENT VIA HW/SW CO-DESIGN PARADIGM

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ABSTRACT

A novel remote sensing (RS) laboratory based on the hardware/software (HW/SW) co-design paradigm for the image enhancement/reconstruction problems pursuing the real time implementation is presented in this study. The application of the developed approach consider the typical single-look synthetic aperture radar (SAR) imaging systems operating in real-world RS scenarios with uncertainties attributed to random signal perturbations in inhomogeneous propagation medium (i.e., possible to imperfect system calibrations and carrier trajectory deviations). The proposed “real time remote sensing laboratory” (RTRSL) provides a HW-level platform for the evaluation of different collaborative RS imaging techniques using the Xilinx Virtex-4 XC4VSX35-10ff668 field programmable gate array (FPGA). Hardware implementation examples are reported to illustrate the usefulness of the developed RTRSL for system-level and algorithmic-level optimization of high-resolution image enhancement tasks performed with the real-world RS imagery.

Index Terms—Remote Sensing; HW/W co-design; FPGA.

1. INTRODUCTION

The optimization of digital and image processing techniques, for the real time enhancement/reconstruction of remote sensing (RS) environmental imagery, is nowadays an important investigation field [1]. Such digital RS images are acquired with the use of high-resolution array radar and synthetic aperture radar (SAR) [2]. In particular, many RS imaging problems require applications with a response in (near) real time in areas such as environmental modeling and assessment, target detection for military and homeland defense/security purposes, and risk prevention and response. The latter includes tracking wildfires, detecting biological threats, and monitoring oil spills and other types of chemical contamination. However, despite the growing interest in RS imaging technology, only a few parallel processing architectures exist in the literature. To provide the high computational demands under real-time constraints; a highly parallel processing scheme has to be applied. Usually, some previous RS techniques have been based on multi-PC or digital signal processing (DSP) platforms [3]–[5].

The innovative contribution of this study consists in develop a “Real Time Remote Sensing Laboratory” (RTRSL) platform based on the hardware/software (HW/SW) co-design paradigm that perform systematic-level implementations of different collaborative RS imaging problems in context of a real time computational mode. The scientific challenge is to develop and investigate via the RTRSL an intelligent signal processing (SP) perspective for the processing of high-resolution RS imaging, search, discovery, discrimination, mapping and problem-oriented analysis of spatially distributed physical remote sensing signature fields. The end-user oriented RTRSL platform is elaborated directly to assist in system-level and algorithmic-level optimization of such multi-sensor collaborative high-resolution image enhancement tasks performed with real-world RS imagery.

2. SUMMARY OF REMOTE SENSING TECHNIQUES

In this section, it is presented a brief summary of the main RS-regularization techniques that were previously developed in [3]. Let us consider the measurement data wavefield $u(y)=s(y)+n(y)$ modeled as a superposition of the echo signals $s$ and additive noise $n$ that assumed to be available for observations and recordings within the prescribed time-space observation domain $Y\{y\}$, where $y=(t,p)^T$ defines the time-space points in the observation domain $Y=T\times P$. The model of observation wavefield $u$ is specified by the linear stochastic equation of observation (EO) of operator form [3]:

$$u=Se+n; \quad e\in E; \quad u,n\in U; \quad S:E\rightarrow U.$$  

Next, we take into account the conventional finite-dimensional vector form approximation of the continuous-form EO.

$$u=Se+n$$  

where $u$, $n$ and $e$ define the vectors composed by the coefficients of the finite-dimensional approximation of the fields $u$, $n$ and $e$, respectively, and $S$ is the matrix-form approximation of the signal formation operator (SFO). The
average $b = \text{vect} \langle c_k, e_k^* \rangle; k = 1, ..., K$ of the random scattering vector $e$ has a statistical meaning of the average power scattering function traditionally referred to as the spatial spectrum pattern (SSP), where the asterisk indicates the complex conjugate. This SSP is a second order statistics of the scattered field that represent the brightness reflectivity of the image scene $B = L \{ b \}$, represented in a conventional pixel format over the rectangular scene frame [3]. The RS imaging problem is stated as follows: to find an estimate of the scene pixel-frame image $\hat{B}$ via lexicographical reordering $\hat{b} = L \{ \hat{b} \}$ of the spatial spectrum pattern (SSP) vector estimate $\hat{b}$ reconstructed from whatever available measurements of independent realizations $\{ u_j \}; j = 1, \ldots, J$ of the recorded data vector.

Thus, one can seek to estimate $\hat{b} = \{ \hat{R} \}_\text{diag}$ given the data correlation matrix $\hat{R}_u$ pre-estimated by some means, e.g. via averaging the correlations over $J$ independent snapshots \[ \hat{R}_u = \text{Y aver} \{ u_j u_j^* \} = (1/J) \sum_{j=1}^J u_j u_j^* \] (2)

and by determining the solution operator that it is also referred to as the signal/image formation operator (SO) $F$ such that

\[ \hat{b} = \{ \hat{R} \}_\text{diag} = \{ FYF \}_\text{diag} \]. \hspace{1cm} (3)

To optimize the search of such SO $F$, it is formulated the following strategy

\[ F = \arg \min_F \{ \mathcal{H}(F) \} \quad \text{subject to:} \quad <\| \Delta \|^2 >_{p(\Lambda)} \leq \delta \] \hspace{1cm} (4)

where the conditioning term represents the worst-case statistical performance (WCSP) regularizing constraint imposed on the unknown second-order statistics $<\| \Delta \|^2 >_{p(\Lambda)}$ of the random distortion component $\Delta$ of the SFO matrix.

The solution to the problem (4) provides the optimal SO as follows

\[ F = K S^+ R_n^{-1}, \quad \text{where} \quad K = (S^+ R_n^{-1} S + \alpha A^{-1})^{-1}. \] \hspace{1cm} (5)

where $\alpha$ is the balance (regularization) parameter, $R_n^{-1}$ is the inverse of the diagonal-form correlation matrix $R_u$, and the weight matrix $A$ provides the additional regularization “degrees of freedom” incorporating any descriptive properties of a solution [3].

A family of the RS-regularized algorithms are derived from (4), (5) via adjusting the regularization parameter $\alpha$ and weight matrix $A$. Such robust methods among them are: the rough conventional matched spatial filtering (MSF) approach [1]; the descriptive maximum entropy (ME) technique [6]; the robust spatial filtering (RSF) method [3], the robust adaptive spatial filtering (RASF) technique [4]; etc. These were detailed in the previous studies [1],[3]–[4], [6]. It is important to note that due to the non-linearity of the optimization problem (3), (4), the solutions typically require extremely complex operations. Therefore, these high computational complexities of the RS-regularized algorithms make them definitely unacceptable for real time PC-aided implementations. To treat such class of RS real time implementations, the use of specialized efficient HW-level array of processors using the HW/SW co-design scheme will become a real possibility for newer high computationally demanded RS applications.

Figure 1. HW/SW co-design scheme.
3. HW/SW CO-DESIGN PARADIGM

The HW/SW co-design is a hybrid method aimed at increasing the flexibility of the implementation and improvement of the overall design process [7].

Two opposite alternatives can be considered when exploring the HW/SW co-design of a complex electronic system. One of them is the use of standard components whose functionality can be defined by means of programming (i.e., DSP platforms). The other one is the implementation of this functionality via very large scale integration (VLSI) circuits, specifically tailored for that application. It is well known that the first alternative (i.e., the SW alternative) provides solutions that present a great flexibility in spite of high area requirements and long execution times, while the second one (i.e., the HW alternative) optimizes the size aspects and the operation speed but limits the flexibility of the solution. Halfway between both, HW/SW co-design technique try to obtain an appropriate trade-off between the advantages and drawbacks of these two approaches.

The main parameters to consider in this study are the task execution speed and the area required by its HW-level implementation. Based on those parameters considerations, the HW/SW co-design methodology is carried out, which consists in deciding which tasks should be executed by SW and which should be implemented by HW; the fixed-point software stage analysis (i.e., for this study is considered the selection of 9 bits integer and 23 fractional bits with rounding to nearest format for all the fixed-point operations) and the C/C++ reference implementation. Notice that the RS acquired images are stored and loaded from a compact flash device and the resulting enhanced images are also stored to the same memory device.

Figure 1 presents the conceptualization of the HW/SW co-design scheme to realize the real time remote sensing laboratory (RTRSL). From the implementation results presented further on in the next section, one can consider that the addressed HW/SW co-design paradigm definitively can approach the real time RS image processing requirements using a Field Programmable Multiprocessor System on Chip (MPSoC) platform while performing the image enhancement of the large-scale real-world RS imagery.

4. REAL TIME REMOTE SENSING LABORATORY

The purpose of the RTRSL platform is to implement in real time HW-level sense the main RS-regularized methods for the image enhancement/reconstruction tasks. The RTRSL software is implemented in a Virtex-4 field programmable gate array (FPGA). The RTRSL offer to the user different options of acquisition and processing of any image in the JPEG, TIFF, BMP and PNG format as a test scene input image from the compact flash memory device. Also, the user can select different system-level effects of image degradation with a particular simulated RS system, simulation of random noising effects with different noise intensities and distributions.

Next, the RS image enhancement tasks are proved in real time efficient mode for different real-world scenarios. As an exemplified test-case, the RSF and RASF algorithms have been employed with the RTRSL. The fixed-point representation of the algorithms RSF and RASF developed at the SW-design are conceptualized and implemented with the MicroBlaze embedded processor and with three specialized HW coprocessors. The first coprocessor, referred to as matched space filter (MSF), implements the calculations to form the MSF image. The second coprocessor, referred to as point spread matrix (PSM), implements the operations of the PSM concurrently over the azimuth and the range directions. The third coprocessor, referred to as the updating module, performs the required robust updating $A^{-1} = \text{diag}^{-1}(\hat{b}_{0n})$ for implementing the RSF algorithm and the adaptive updating $A^{-1} = \text{diag}^{-1}(\hat{b}_{on})$ for implementing the RASF image enhancement algorithm, respectively.

Once the HW/SW co-design has been defined, the three coprocessors employed in the architecture are implemented using the HW processors arrays (PAs). A PA consists of a network of processor elements (PEs) interconnected with local data communications among the PEs in order to achieve the maximum possible parallelisms in the computations and decreasing the area and time processing of the scheme presented in Figure 1. Also, the implementation of parallel computing techniques based on Polytope transformations [7] have been used to improve the performance the coprocessor architectures.

A. Implementation Results

The test-case experiments of the RTRSL, reported in this paper, are related to the enhancement of the RS images acquired with different fractional SAR systems characterized by the PSF of a Gaussian "bell" shape in both directions of the 2-D scene (in particular, of 16 pixel width at 0.5 from its maximum for the 512-by-512 BMP pixel-formatted scene). The images are stored and loaded from a compact flash device for the image enhancement process, i.e., particularly for the RSF and RASF techniques. The initial test scene is displayed in Figure 2 (a). Figure 2(b) presents the same original image but degraded with the matched space filter (MSF) method. The qualitative HW results for the RSF and RASF enhancement/reconstruction procedures are shown in Figures 2(c) and 2(d) with the corresponding IOSNR (improvement in the output signal-to-noise ratio [1], [4]) quantitative performance enhancement metrics reported in the figure captions (in the [dB] scale).
Figure 2. RTRSL results for SAR images with the at 15dB of SNR: (a) Original test scene; (b) degraded MSF-formed SAR image; (c) RSF reconstructed image (IOSNR = 6.56 dB); (d) RASF reconstructed image (IOSNR = 8.72 dB).

B. Performance Analysis

In this sub-section, the comparative analysis of the HW-level specialized coprocessors using the Xilinx Virtex-4 FPGA is next presented. The achieved HW-level architecture is constructed following the addressed HW/SW co-design approach. The synthesis metrics related to the implementation of the PAs architectures as coprocessors are summarized in Table 1. The parameters of the MSF, PSM and updating coprocessor modules are specified as follows: data matrices of size 32×32 and two Band-Toeplitz PSF matrices of the same 12×12 pixel size width. Last, it is compared the achieved processing time of the RTRSL using the HW/SW co-design paradigm as reported in Table 2. First, the conventional MATLAB reference implementation of the RSF/RASF algorithms were implemented in a personal computer (PC) running at 1.73GHz with a Pentium (M) processor and 1GB of RAM memory. In the second case, the same RSF/RASF algorithms were implemented using the proposed HW/SW co-design architecture with the FPGA platform.

5. CONCLUSION

The presented study provides a RS laboratory via the HW/SW co-design paradigm for the evaluation of different collaborative RS imaging techniques in context of their real time implementation as required for environmental resource management with the use of multi-sensor RS data. To accomplish such computationally complex requirements, the developed of a RTRSL platform is composed of specialized HW coprocessors based on PAs for the analysis and implementation of image enhancement/reconstruction techniques. The reported HW-level implementation results of Tables 1 and 2 are illustrative of the RTRSL usefulness and capabilities in context of their real time operational mode for different RS imaging tasks performed with real-world RS images.

6. REFERENCES